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10/075,868	02/13/2002	Josef Schmid	3	9427

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Docket Administrator (Room 3J-219)
Lucent Technologies Inc.
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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	4

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/075,868	**Applicant(s)** SCHMID, JOSEF	
	Examiner John J. Tabone, Jr.	**Art Unit** 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been examined.

Drawings

2. Figures 1, 2 and 4 are objected to as failing to comply with 37 CFR 1.84(o). All features must be labeled with a function that indicates what element the boxes represent. No new matter should be entered.

3. Figures 1 and 2 are objected to because of hanging signal lines with no label assigned to them. No new matter should be entered.

4. Figure 3 is objected to due to a typographical error on label TD/DCO. This should be TDO/DCO. No new matter should be entered.

5. The Applicant is advised that corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawings sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required

corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities: Page 5, line 17 has a typographical error „ quality level". This should be corrected to "quality level". Appropriate correction is required.

Claim Objections

7. Claims 1, 8 and 18 are objected to according 37 C.F.R. § 1.75(i) which states: Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. The indentations should replace the hyphens. Appropriate correction is required.

8. Claims 1, 15, 18 and 19 are objected to because of the following informalities:

Claim 1:

This claim is missing a comma at the end of line 6. Appropriate correction is required.

Claim 15:

This claim has a typo on output pot (DCO). The Examiner interprets this as output port (DCO). Appropriate correction is required.

Claim 18:

This claim is missing a semi-colon at the end of line 3. Appropriate correction is required.

Claim 19:

The claim limitation "step of entering comprises" should be changed to reflect the step of entering which is disclosed. This should read "step of entering a delay measurement mode comprises". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 10, 12 and 18-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10:

This claim recites the limitation "the combinational bypass path (BP)" on lines 1 and 2. There is insufficient antecedent basis for this limitation in the claim. Also, this claim has inconsistent use of a term with claim 8.

Claim 12:

This claim recites the limitation "the bypass path (BP)" on line 1. There is insufficient antecedent basis for this limitation in the claim. Also, this claim has inconsistent use of a term with claim 8.

Claim 18:

The reciting the limitation "a port (TDO, DCO)" on line 7 make the claim indefinite because "a port" is a single port where "(TDO, DCO)" is plural. For purpose of examination the Examiner will read the limitation as "a port (TDO)". Further clarification is required.

Claims 19-21:

These claims are also rejected because they depend on claim 18 and have the same problems of indefiniteness.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-5, 8-13, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Jacobson et al. (US-6314539), hereinafter Jacobson.

Claim 1:

Jacobson teaches BSR cell 800 includes a test data input (TDI) terminal (SI), a SYSTEM DATA IN terminal, an input multiplexer (MUX) 810, a shift register flip-flop 820 (a storage layer between a scan input port (SI) and a scan output port (SO)), a test data output (TDO) terminal (SO), a parallel latch 830, an output MUX 840 and a SYSTEM DATA OUT terminal. (Col. 9, lines 59-63). Jacobson also teaches bypass MUX 850 includes a first input terminal connected to the TDI terminal, a second input terminal connected to the output terminal of shift register flip-flop 820, and an output terminal

connected to the TDO terminal that is used to shift data signals along the BSR. Jacobson further teaches when select control circuit 855 transmits a second (e.g., low) signal (analyzing each scan cell to identify a redundant state), bypass MUX 850 passes signals directly from the TDI terminal, thereby bypassing input MUX 810 and shift register flip-flop 820, effectively by programming bypass MUX 850 to pass data signals directly from the TDI terminal to the TDO terminal (creating an additional combinational path (BP) between the scan input port (SI) and a scan output port (SO)). (Col. 10, lines 15-29). Jacobson even further teaches PLD 1100 is configured to perform Boundary-Scan Test procedures where BSR cells that are used by neither first logic function 1118(A) nor second logic function 1118(B) are effectively removed from the BSR by programming the bypass circuits of these BSR cells to pass signals directly from their TDI terminals to their TDO terminals (implementing each scan cell in the integrated circuit by creating said scan chain). (Col. 13, lines 22-29, FIG. 11A).

<u>Claim 8:</u>

Jacobson teaches BSR cell 800 includes a test data input (TDI) terminal (<u>scan input port (SI)</u>), a SYSTEM DATA IN terminal (<u>input port (PI)</u>), an input multiplexer (MUX) 810, a shift register flip-flop 820 (a finctional layer), a test data output (TDO) terminal (<u>scan output port (SO)</u>), a parallel latch 830, an output MUX 840 and a SYSTEM DATA OUT terminal (<u>output port (PO)</u>). (Col. 9, lines 59-63). Jacobson also teaches bypass MUX 850 includes a first input terminal connected to the TDI terminal, a second input terminal connected to the output terminal of shift register flip-flop 820, and an output terminal connected to the TDO terminal that is used to shift data signals along

the BSR. Jacobson further teaches when select control circuit 855 transmits a second (e.g., low) signal, bypass MUX 850 passes signals (combinational path (BP) between the scan input port (SI) and the scan output port (SO) bypassing said storage layer) directly from the TDI terminal, thereby bypassing input MUX 810 and shift register flip-flop 820, effectively by programming bypass MUX 850 to pass data signals directly from the TDI terminal to the TDO terminal (creating an additional combinational path (BP) between the scan input port (SI) and a scan output port (SO)). (Col. 10, lines 15-29).

Claim 12:

Jacobson teaches a PLD 1100 that is configured to perform Boundary-Scan Test procedures where BSR cells that are used by neither first logic function 1118(A) nor second logic function 1118(B) are effectively removed from the BSR by programming the bypass circuits of these BSR cells to pass signals directly from their TDI terminals to their TDO terminals (connecting the scan input port (SI) of a first scan cell to a test data input port (TDI) for boundary scan testability and the scan output port (SO) of a scan cell forming the end of the scan chain via a test data output path (BSR_TDO) to a test data output port (TDO) for boundary scan testability). Jacobson also teaches the variable length BSR of PLD 1100 has an effective length of 10 BSR cells, which is less than half of the maximum length (27 BSR cells) of the BSR where the reduced-length BSR facilitates significantly faster Boundary-Scan Test procedures (a boundary scan chain having delay measurement functionality) over conventional fixed-length BSRs because significantly less data is required. (Col. 13, lines 22-51, FIG. 11A).

Claim 18:

Jacobson teaches when select control circuit 855 transmits a second (e.g., low) signal (entering a delay measurement mode), bypass MUX 850 passes signals directly from the TDI terminal, thereby bypassing input MUX 810 and shift register flip-flop 820, effectively by programming bypass MUX 850 to pass data signals directly from the TDI terminal to the TDO terminal. (Col. 10, lines 15-29). Jacobson also teaches that the TDI signal is used for serial transmission of data or instruction bits, depending upon the state of TAP controller 220 (applying a test data signal on a test data input (TDI) for boundary scan testability). (Col. 3, lines 59-61). Jacobson further teaches the PLD 1100 is configured to perform Boundary-Scan Test procedures where BSR cells that are used by neither first logic function 1118(A) nor second logic function 1118(B) are effectively removed from the BSR by programming the bypass circuits of these BSR cells to pass signals directly from their TDI terminals to their TDO terminals (BSR_TDO). Jacobson even further teaches the variable length BSR of PLD 1100 has an effective length of 10 BSR cells, which is less than half of the maximum length (27 BSR cells) of the BSR where the reduced-length BSR facilitates significantly faster Boundary-Scan Test procedures (performing the delay measurement at a port (TDO) connected to the test data output path (BSR_TDO) for scan testability) over conventional fixed-length BSRs because significantly less data is required. (Col. 13, lines 22-51, FIG. 11A).

Claims 2 and 9:

Jacobson teaches in FIG. 2 a detailed block diagram showing an example of the basic hardware elements provided on an IEEE Standard 1149.1 compliant PLD where the basic hardware elements include a test access port (TAP) 210, a TAP controller

220, an instruction register (IR) 230, an instruction decode circuit 235, a test data register circuit 240, an output multiplexer (MUX) 250, an output flip-flop 260 and a tri-state buffer 270. Jacobson also teaches TAP 210 provides access to the test support functions build into an IEEE Standard 1149.1 compliant PLD and includes three input connections for receiving the test clock input (TCK) signal, the test mode select (TMS) signal, and the test data input (TDI) signal (providing of the at least one boundary scan cell according to the IEEE Standard 1149.1). (Col. 3, lines 43-61).

Claim 3:

Jacobson teaches bypass MUX 850 includes a first input terminal connected to the TDI terminal, a second input terminal connected to the output terminal of shift register flip-flop 820, and an output terminal connected to the TDO terminal that is used to shift data signals along the BSR. Jacobson also teaches when select control circuit 855 transmits a second (e.g., low) signal, bypass MUX 850 passes signals directly from the TDI terminal, thereby bypassing input MUX 810 and shift register flip-flop 820, effectively by programming bypass MUX 850 to pass data signals directly from the TDI terminal (SI) to the TDO terminal (SO) (creating an additional combinational path comprises the step of implementing a local path (BP) between said respective two scan ports (SI, SO) by bypassing the respective storage layer of a boundary scan cell). (Col. 10, lines 15-29).

Claims 4 and 10:

Jacobson teaches bypass MUX 850 includes a first input terminal connected to the TDI terminal, a second input terminal connected to the output terminal of shift

register flip-flop 820, and an output terminal connected to the TDO terminal that is used to shift data signals along the BSR. Jacobson also teaches when select control circuit 855 transmits a second (e.g., low) signal, bypass MUX 850 passes signals directly from the TDI terminal, thereby bypassing input MUX 810 and shift register flip-flop 820, effectively by programming bypass MUX 850 to pass data signals directly from the TDI terminal to the TDO terminal (combinational path is connected to the scan output port (SO) via a multiplexer (MUX) controlled by the shift signal from a test access port controller). (Col. 10, lines 15-29).

<u>Claims 5 and 13:</u>

Jacobson teaches a PLD 1100 that is configured to perform Boundary-Scan Test procedures where BSR cells that are used by neither first logic function 1118(A) nor second logic function 1118(B) are effectively removed from the BSR by programming the bypass circuits of these BSR cells to pass signals directly from their TDI terminals to their TDO terminals (<u>connecting the scan input port (SI) of a first scan cell to a test data input port (TDI) for boundary scan testability and the scan output port (SO) of a scan cell forming the end of the scan chain via a test data output path (BSR_TDO) to a test data output port (TDO) for boundary scan testability</u>). (Col. 13, lines 22-29, FIG. 11A).

<u>Claim 11:</u>

Jacobson teaches bypass MUX 850 (<u>the bypass path (BP) comprises at least one additional inverter, library and/or delay element</u>) includes a first input terminal connected to the TDI terminal, a second input terminal connected to the output terminal

of shift register flip-flop 820, and an output terminal connected to the TDO terminal that is used to shift data signals along the BSR. (Col. 10, lines 15-29).

Claim 19:

Jacobson teaches TAP controller 220 is initialized to a Test-Logic Reset state 301 at power up. In this state all test logic is disabled (i.e., all core logic of the PLD operates normally) and will enter Test-Logic Reset state 301 from any other state when TMS is held high (logic 1) for at least five TCK pulses. Jacobson also teaches from Test-Logic Reset state 301, TAP controller 220 enters a Run-Test/Idle state 302 when TMS is held low (logic 0) for at least one TCK pulse and is placed in this state while self-test or data scan operations are performed (step of entering comprises the step of entering a test-logic-reset-state), and remains in this state until TMS is held high.

Claim 20:

Jacobson teaches the variable length BSR of PLD 1100 has an effective length of 10 BSR cells, which is less than half of the maximum length (27 BSR cells) of the BSR where the reduced-length BSR facilitates significantly faster Boundary-Scan Test procedures (performing the delay measurement at the test output port (TDO) for boundary scan testability) over conventional fixed-length BSRs because significantly less data is required. (Col. 13, lines 22-51, FIG. 11A).

11. Claims 6, 14-17, 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Jacobson et al. (US-6314539), hereinafter Jacobson, in view of Whetsel (5710779), hereinafter Whetsel.

Claims 6 and 14:

Jacobson does not explicitly teach connecting the output port (SO) of a boundary scan cell forming the end of the scan chain to a separate delay chain output port (DCO). However, Jacobson does teach that the PLD 1100 is configured to perform Boundary-Scan Test procedures where BSR cells that are used by neither first logic function 1118(A) nor second logic function 1118(B) are effectively removed from the BSR by programming the bypass circuits of these BSR cells to pass signals directly from their TDI terminals to their TDO terminals (BSR_TDO). (Col. 13, lines 22-29, FIG. 11A). Whetsel teaches the use of an additional test output pin (or terminal) TO is added to the IC to output data (a separate delay chain output port (DCO)) during observation and bypass modes of a selected scan path where the TO pin is 3-state (controlled by signal CTL) so that multiple ICs can have a bussed TO connection at the board level. (Col. 5, 26-31, FIG. 13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jacobson's TDO output to add Whetsel's test output pin (or terminal) TO. The artisan would have been motivated to do so because the additional test output terminal TO would enable Jacobson to control the delay chain output with the 3-state buffer.

Claim 15:

The motivation to modify Jacobson's TDO output to add Whetsel's test output pin (or terminal) TO is outlined according to claims 6 and 14 above. Jacobson teaches according to the state of the MODE TEST/NORM control signal, output MUX 840 either passes SYSTEM data (during normal operation) or the contents of parallel latch 840

(during Boundary-Scan Test procedures) to the SYSTEM DATA OUT terminal (TDO). (Col. 10, lines 33-52). Whetsel teaches the TO pin is 3-state (controlled by signal CTL) (test mode signal TM). (Col. 5, 26-31, FIG. 13).). It would have been obvious to one of ordinary skill in the art at the time the invention was made to control Whetsel's 3-state test output terminal with Jacobson's MODE TEST/NORM control signal. The artisan would have been motivated to do so because enable the controlling of the delay chain output with the 3-state buffer.

Claim 16:

Jacobson teaches according to the state of the MODE TEST/NORM control signal, output MUX 840 either passes SYSTEM data (during normal operation) or the contents of parallel latch 840 (during Boundary-Scan Test procedures) to the SYSTEM DATA OUT terminal (TDO). (Col. 10, lines 33-52).

Claim 17:

Jacobson teaches the BSR cell 800 is incorporated into the Boundary Scan architecture of a host IC (electrical device comprising an Integrated circuit) that is similar to that shown in FIG. 2. (Col. 9, lines 55, 56).

Claim 21:

The motivation to modify Jacobson's TDO output to add Whetsel's test output pin (or terminal) TO is outlined according to claims 6 and 14 above. Jacobson teaches the variable length BSR of PLD 1100 has an effective length of 10 BSR cells, which is less than half of the maximum length (27 BSR cells) of the BSR where the reduced-length BSR facilitates significantly faster Boundary-Scan Test procedures (performing the

delay measurement at a port (DCO)) over conventional fixed-length BSRs because significantly less data is required. (Col. 13, lines 22-51, FIG. 11A).

12. Claim 7 is rejected under 35 U.S.C. 102(e) as being anticipated by Jacobson et al. (US-6314539), hereinafter Jacobson, in view of Abadir et al. (US-2002/0112213), hereinafter Abadir.

Claim 7:

Jacobson does not explicitly teach the combinational path (BP) is defined as a false path during synthesizing of the scan chain. Abadir teaches a design analysis tool and method of use for false timing path identification for industrial circuits, both on the integrated circuit (IC) scale as well as a board level. (Page 4, ¶21). It would have been obvious to one of ordinary skill in the art at the time the invention was made use Abadir's design analysis tool and method to synthesize Jacobson's boundary scan circuit to set false path information for the combinational path (BP). The artisan would have been motivated to do so because, as a result of Abadir's design analysis tool and method, engineering resources could be preserved by minimizing wasteful efforts spent on optimizing false timing paths. Furthermore, the artisan would have been motivated to do so because Abadir's design analysis tool and method eliminates the creation of unnecessary circuit area, the dissipation of additional power, and reduction in performance which is typically associated with the optimization of false paths.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Huang (US-5477545)

Huang teaches scan cell for use in a boundary scan test which includes a bypass MUX and a method of using it. (claims 1-5, 8-13, and 18-20).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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